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10EC45

Fourth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain VHDL and verilog? Evaluate the expression E = (A and not B or C or 2 and D) where A = "11", B = "1111", C = "011000", D = "111011" **(07 Marks)**

b. Explain the following data–types:
i) Physical data types ii) User-defined data type iii) Array type iv) Nets and v) Parameters. **(10 Marks)**

c. Write a verilog code for the circuit given in Fig. Q1 (c), using switch level description. **(03 Marks)**

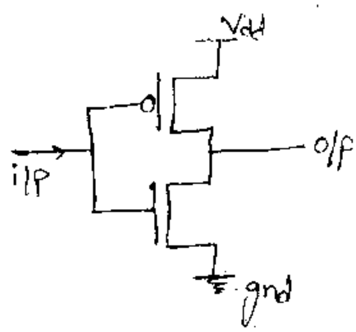

Fig. Q1 (c)

2 a. Explain concurrent execution. **(03 Marks)**

b. Write a verilog code in data flow description for a 2-bit magnitude comparator with the help of truth table and simplified Boolean expressions. **(10 Marks)**

c. Write a VHDL code for 3-bit parallel subtractor using 1-bit full adder in data flow modeling style. **(07 Marks)**

3 a. Compare signal with variable. Give an example for each. **(04 Marks)**

b. Using Booth algorithm, find the product of two signed 4-bit numbers –3 and 5. Write a verilog code using behavioral style of description. **(10 Marks)**

c. Write a VHDL code to determine the number of one's in an 8-bit vector. The output of the detector must be '0' for even number of one's, while '1' for odd number of one's. **(06 Marks)**

4 a. Explain binding between library and module. **(02 Marks)**

b. Write a verilog code to implement S-R latch in structured description. **(06 Marks)**

c. Define state machine using the state machine concept, showing all the details design a counter, which counts 0, 2, 3, 5, 7. Write the VHDL code for the same. (Use JK flip-flop). **(12 Marks)**

PART – B

5 a. What are the significance of procedure, task and functions? Bring out the difference between procedure, task and function with an example. **(08 Marks)**

b. Write a code to convert the fraction binary (4-bit) to real using procedure. **(08 Marks)**

c. Write a note on verilog file processing. **(04 Marks)**

6 a. With syntax, explain package declaration and package body. **(04 Marks)**

b. Write a verilog code to find the greatest element of an array. **(06 Marks)**

c. Write a VHDL code to describe the finite sequential state machine given in Fig.Q6 (c). **(10 Marks)**

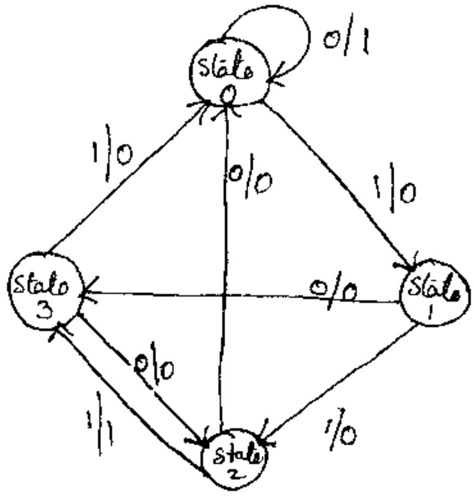

Fig. Q6 (c)

7 a. Write mixed-language description of a master slave D flip flop invoking VHDL entity from a verilog module. **(10 Marks)**

b. Write mixed-language description of a simple JK flip flop with active low clear. **(10 Marks)**

8 a. Define synthesis. Synthesize the VHDL code given in the Fig. Q8 (a)

```
entity Ex is
        Port (a : in natural range 0 to 7;
              Y : out integer range 0 to 15);
end Ex;
architecture Ex1 of Ex is
begin
        Process (a)
          Variable temp : integer range 0 to 15;
        begin
            if (a<3) then temp : = 15;
            elseif (a > = 5) then temp : = 0;
            else
                temp : = a * (-5) + 25;
            end if;
        end process;
end Ex1;
```

Fig. Q8 (a) **(10 Marks)**

b. Write verilog code for signal assignment statement y = 2 * x + 3. Show the synthesized logic symbol and gate level diagram. **(10 Marks)**

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